Remarks

The amendments which have been amended are in accordance with the specification and the drawings of the present invention. Hence, there is no new matter introduced.

In view of the above amendments and the following remarks, reconsideration of the present patent application is respectfully requested.

Regarding Claims 11-14:

Claims 11-14 are rejected under 35 U.S.C. 102 as being unpatentable over Fukumoto's invention (US Patent 5,753,953). The applicant respectfully traverses the rejection.

The claimed invention according to claim 11 comprises a cell size smaller than the traditional split-gate structure without sacrificing program disturb immunity.

The applicant respectfully submits that the claimed invention solves a problem that the cited reference fails to solve, but also does not even acknowledge.

The applicant respectfully points out that the claimed invention discloses a floating gate self-aligned to one side of the select gate, wherein the lengths of the floating gate and the select gate can be controlled more precisely than in a non-self-aligned process. Thus, the memory cell according to the present invention has a cell size smaller than the traditional split gate structure without sacrificing program disturb immunity, as noted for example at page 8, line 5. Moreover, the problem current of the memory cell according to

the present invention is much lower than the stack-gate structure because it is programmed by using source side injection.

In the Office Action, the Fukumoto reference is characterized as disclosing an EEPROM device (Fig. 1) comprising a silicon substrate 1 having a source/drain region 2, a tunnel oxide layer 4 disposed over the silicon substrate 1, a select gate 6 disposed over the tunnel oxide layer 4, wherein the select gate 6 is defined by conductive layer covered with a first insulated material 8a thereon and comprises a sidewall 8 made of a second insulated material, a floating gate 7 aligned to two sides of the select gate 6, a third insulated material 10 disposed over the tunnel oxide layer, the select gate and the floating gate, and a control gate 9 formed on the third insulated material. As is readily apparent, the Fukumoto fails to teach or suggest a floating gate aligned to one side of the select gate.

In the claimed invention, the floating gate is self-aligned to one side of the select gate. This is done to reduce the cell size of an Electrically Erasable Programmable Read-Only Memory (EEPROM). This makes the claimed invention potentially distinct from the cited reference.

For example, in Fig. 1 of Fukumoto, two traditional floating gates 7 respectively aligned to two sides of the select gate 6 are disclosed. In the present invention, a completely different structural arrangement is claimed. Claim 11 requires that the **floating gate be aligned to one side of the select gate.** Obviously, the claimed invention

discloses a different Electrically Erasable Programmable Read-Only Memory (EEPROM) as compared to the device disclosed in Fukumoto.

The junctions 2 and 3 of Fukumoto are not similar to the junctions 113 and 114 of the present invention. In the present invention, the depths of the junctions 113 and 114 are the same. Although the depths of the junction 2 and 3 in Fig. 1 of the cited invention seem to the same, actually, the junction 2 and 3 should have different depths because the junction 3 has to be much more deeper than junction 2 to make the junction 3 extend to the region under gate 6. Usually the lateral junction extension is about 0.7 times the depth of the junction. As a result, the cell size scaling becomes more difficult because of the deeper junction 3.

Comparing Fig. 1 of the Fukumoto with the present invention, the memory of the cited invention further comprises the right-side spacer (the additional floating gate 7). The additional floating gate 7 occupies an additional space. Thus the cell size has to be increased. Although the right-side spacer has no practical need in Fukumoto's invention, the inclusion of a right-side spacer makes the disclosed device unable to achieve small cell size. In the present invention, the right-side spacer is removed, and thus makes the depths of the junctions 113 and 114 the same. As a result, the cell of the present invention is much easier for device scaling.

As the claimed invention according to claim 14 comprises steps and/or functionality neither disclosed nor even suggested by those cited references, the applicant respectfully

submits that claims 1 and 14 are not obvious from Liu in view of Sengupta and further in view of Chang. Reconsideration and withdrawal of the rejection is respectfully requested.

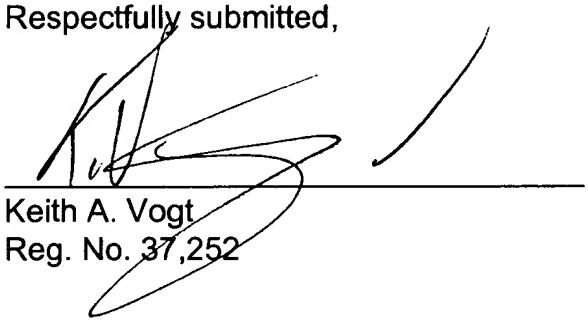
Claims 12-14 depend from claim 11, and incorporate the limitations thereof. The remarks made above with regard to claim 11 apply equally to these dependent claims. The applicant respectfully submits that separate arguments need not be presented in support of these dependent claims at this time. The applicant does not concede the correctness of the rejection, and reserves the right to present further arguments against it.

Although the Examiner cites Fukumoto's invention in the Office Action, the present invention is certainly patentable over the cited references. After reviewing the cited references, it is believed the claims 11-14 of the present patent are certainly patentable over the prior documents under not only 35 U.S.C. 102 but also 35 U.S.C. 103.

CONCLUSION

After comparing the contrasted technical features, claims 11-14 of the present invention are considered to be patentable under 35 U.S.C. 102 and 35 U.S.C. 103 in view of the cited reference. According to the descriptions of the present invention and the cited patent, it is easy to distinguish significant differences between the present invention and the cited prior art. It is believed that the cited reference fails to disclose or teach the present invention as described in the above descriptions.

Respectfully submitted,



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Marked- Up Copy of Claims

11. A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon substrate having a source/drain region;

a tunnel oxide layer disposed over said silicone substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a floating gate aligned to one side of said select gate;

a third insulated material disposed over said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material.

AMENDED ABSTRACT

The present invention concerns the structure of a self-aligned split-gate EEPROM memory cell. The memory cell has a cell size smaller than the traditional split-gate structure without sacrificing program disturb immunity and includes a silicon substrate having a source/drain region, a tunnel oxide layer disposed over the silicone substrate, a select gate disposed over the tunnel oxide layer. The select gate is defined by a conductive layer covered with a first insulated material and includes a sidewall made of a second insulated material, a floating gate aligned to the select gate, a third insulated material disposed over the tunnel oxide layer, the select gate and the floating gate, and a control gate formed on the third insulated material.